**Introduction: -**

Reliability of electronic circuits, which has always been an important issue, is becoming an increasing concern due to the ongoing downscaling of the structural dimensions and the continuous increase in performance requirements. (Lienig & Scheible, 2020).

All integrated circuits contain electrical elements not required for their operation. These include reverse-biased isolated junctions, and resistances and capacitances between various diffusions and depositions. The circuit does not benefit from the presence of these parasitic components, but they can negatively affect its operation sometimes.

***Nothing in an integrated circuit operates perfectly.*** An IC is built of layers. You have metals running over other metals. You have transistors next to other transistors. You have transistors built in substrates. Whenever you introduce two different materials like this, you end up creating extra capacitances. It’s like we deliberately placed lots of tiny capacitors all over our circuit. And worst of all, we cannot get rid of them. (Saint & Saint, 2002).

Sensitive circuitry may be subjected to noise, for instance, through capacitive coupling. This section will talk about parasitic devices that cause junctions, which are typically reverse-biased, to become forward biassed. When the forward bias of these junctions is applied, current starts to flow between circuit nodes that are typically kept apart. These leakages may only cause minor parametric shifts if these currents are small and the circuit is relatively insensitive to their presence. The circuit's functionality may be catastrophically damaged by larger currents. Even after the triggering event has been removed, the malfunctioning circuit may latch up and continue to act improperly. Because latchup generates excessive power dissipation and consequent overheating, an integrated circuit may actually be physically destroyed. Even if the circuit does not self-destruct, it can only be brought back to normal operation by cutting the power. (Hastings, 2001, p. 139)

**Chapter contents:**

* Parasitic capacitance
* Parasitic resistance
* Parasitic inductance
* Interconnect Parasitics
* Overvoltage Protection
* Migration Effects in Metal

1. **Parasitic capacitance (3)**
   1. **Where do parasitics come from?**

You can find them everywhere, really. As we said earlier, every time you run a wire or you run a gate stripe or you create anything in a chip, you get some kind of parasitic. (Saint & Saint, 2002).

To illustrate how prevalent parasitics can be, let’s look at four metal traces above two other metal traces small blue boxes In Fig. 3.1. Between each of these wires, there is effectively a parallel plate capacitor. There is also a capacitance from each of the four wires down to the lower layer, and from the *lower layer to the substrate*. We also have the *fringe capacitances* all the way down. Every little piece of your circuit speaks to every other little piece of your circuit, through some kind of a capacitance.

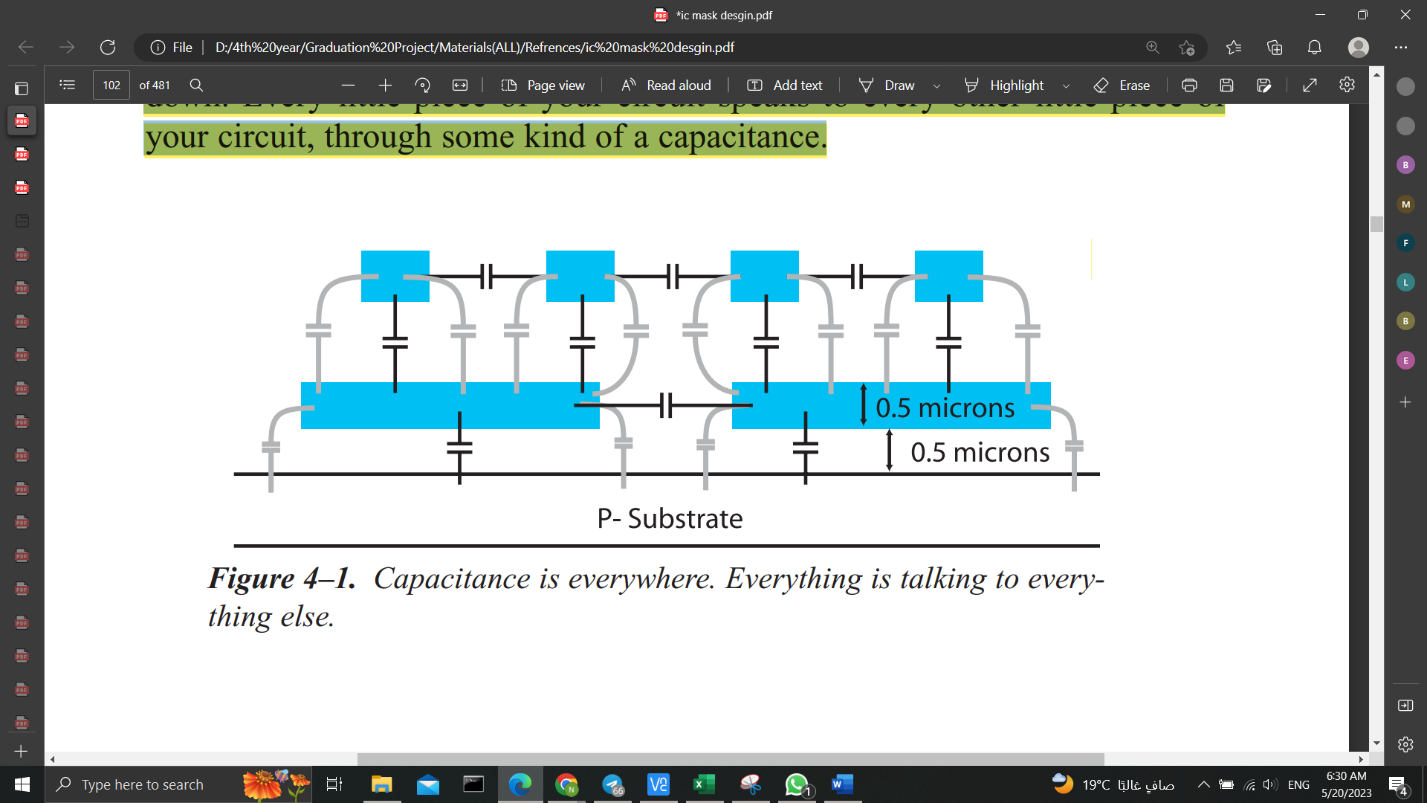


Figure. 3.1. Capacitance is everywhere. Everything is talking to everything else.

But if you have a circuit that is very insensitive to capacitance, let us say like a power regulator, or something else that is quite hefty in the circuit, then you really do not care about these little extra capacitances all over the place.

However, the faster you go, the higher the frequency, the higher the speed of the circuit you are trying to work with, the more important these capacitances become. They do matter.

***Ignoring parasitics can kill your chip.*** In most circuits, if you do not pay attention to parasitics, then the parasitics can kill your chip. Typically, when you do analog layout, whether it’s CMOS or Bipolar “it is CMOS in the new technology”, if there is any reasonably high frequency involved, maybe 20 megahertz or higher, you will have to worry about parasitics of some sort.

* 1. **Techniques to handle the capacitance:**
* Wire Length

When you reduce the length of the wire, then you are reducing the overlap between the wire and substrate, or the wire and something else that happens to be conducting.

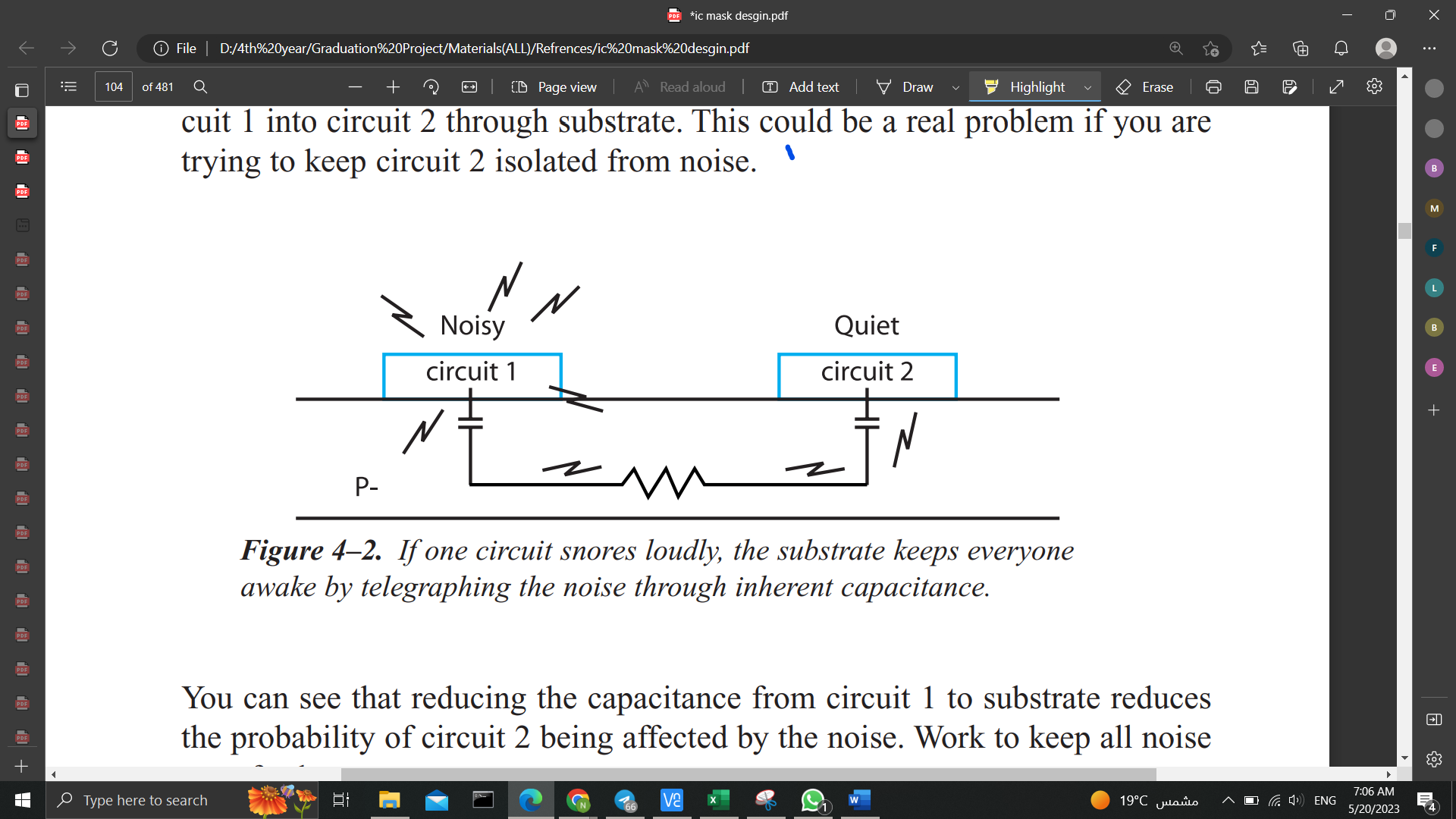
Imagine that you are told some areas of wiring need to be low parasitic, then one of the easiest ways to accomplish that is to keep the wire as short as possible, as mentioned above.

* Metal Selection

Another solution depends on the metal system that you have available to you. And that is since the type of the metals used in the layout are sometimes is decided by the manufacturer.

The dominant capacitance issue is usually the capacitance of the wire going down to substrate. That capacitance is the one you are most interested in as substrate goes everywhere. It runs under the entire chip” the black board in the CAD tools is literally a p-substrate”, so any announcement made to substrate is carried to every other component.

As we can see in fig. 3.2, two circuits, each placed in a P-substrate. You can also see that each circuit has a capacitance to substrate. We also have the parasitic resistance of the substrate itself. The parasitics can couple the noise from circuit 1 into circuit 2 through substrate. This could be a real problem if you are trying to keep circuit 2 isolated from noise.



*Figure. 3.2. If one circuit snores loudly, the substrate keeps everyone awake by telegraphing the noise through inherent capacitance*.

Depending on our metal processing, a second way to reduce parasitics is to use the highest-level metal, the metal furthest away from the substrate. Typically, the further we get from substrate the less capacitance we have because the distance between the two plates is a lot further. *Capacitance is inversely proportional to the distance between plates*, like other types of radiation. A little distance makes a lot of difference.

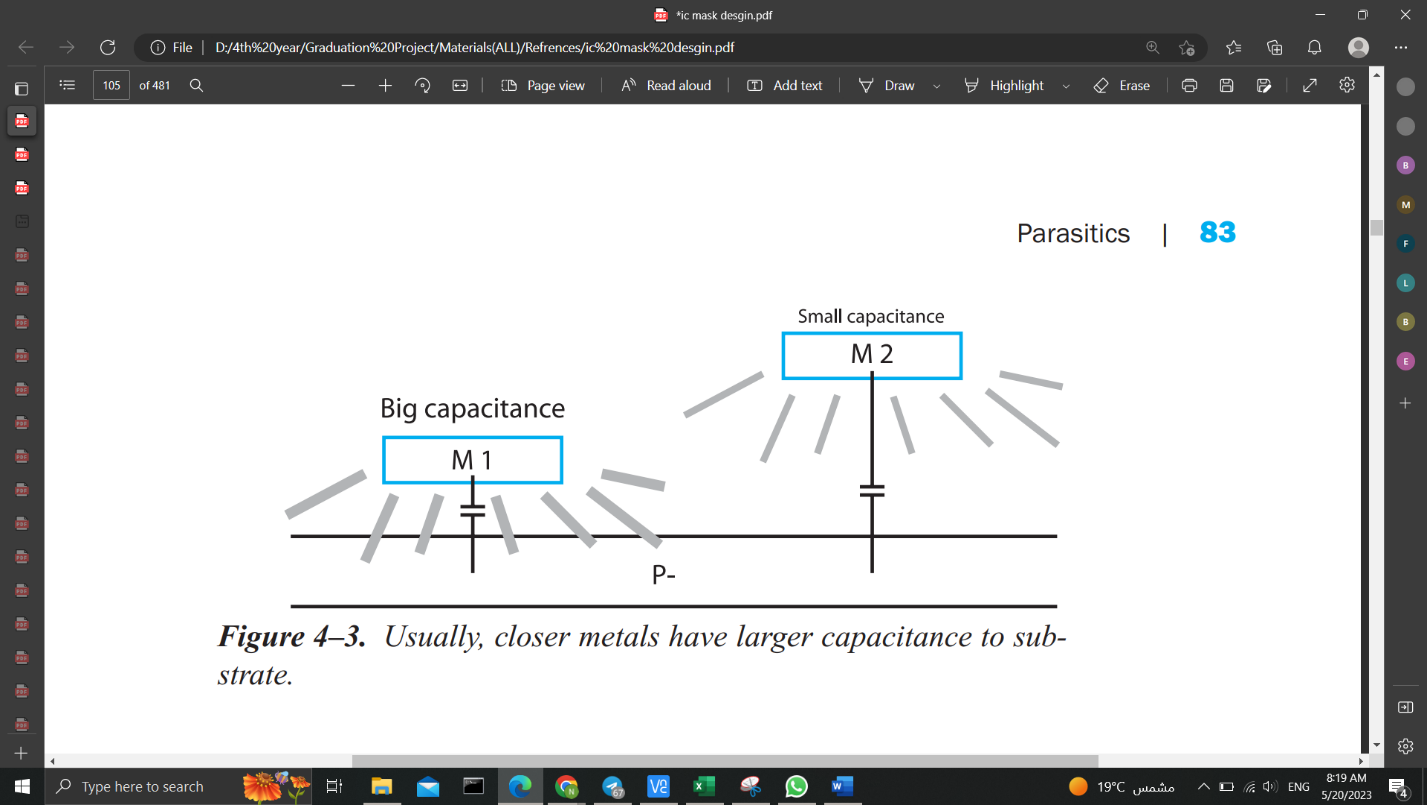


Figure. 3.3. Usually, closer metals have larger capacitance to substrate

But unfortunately, by just saying that the highest-level metal has the least capacitance is not always true. This is where our particular metal processing could make a difference.

The design rules of the metals may conspire against us. So, we have to look carefully through our process manual to calculate which metal is the lowest capacitance, mainly since the minimum width of these metals may be unique. ***Calculate, don’t assume.***

* Metal over Metal

Up to this point, we have been talking about capacitance to substrate. As we mentioned at the start of the chapter, there are capacitances from everything to everything. For example, consider a circuit with a wire that runs over the top of another circuit. Parasitic capacitance develops between that wire and everything in the underlying circuit.

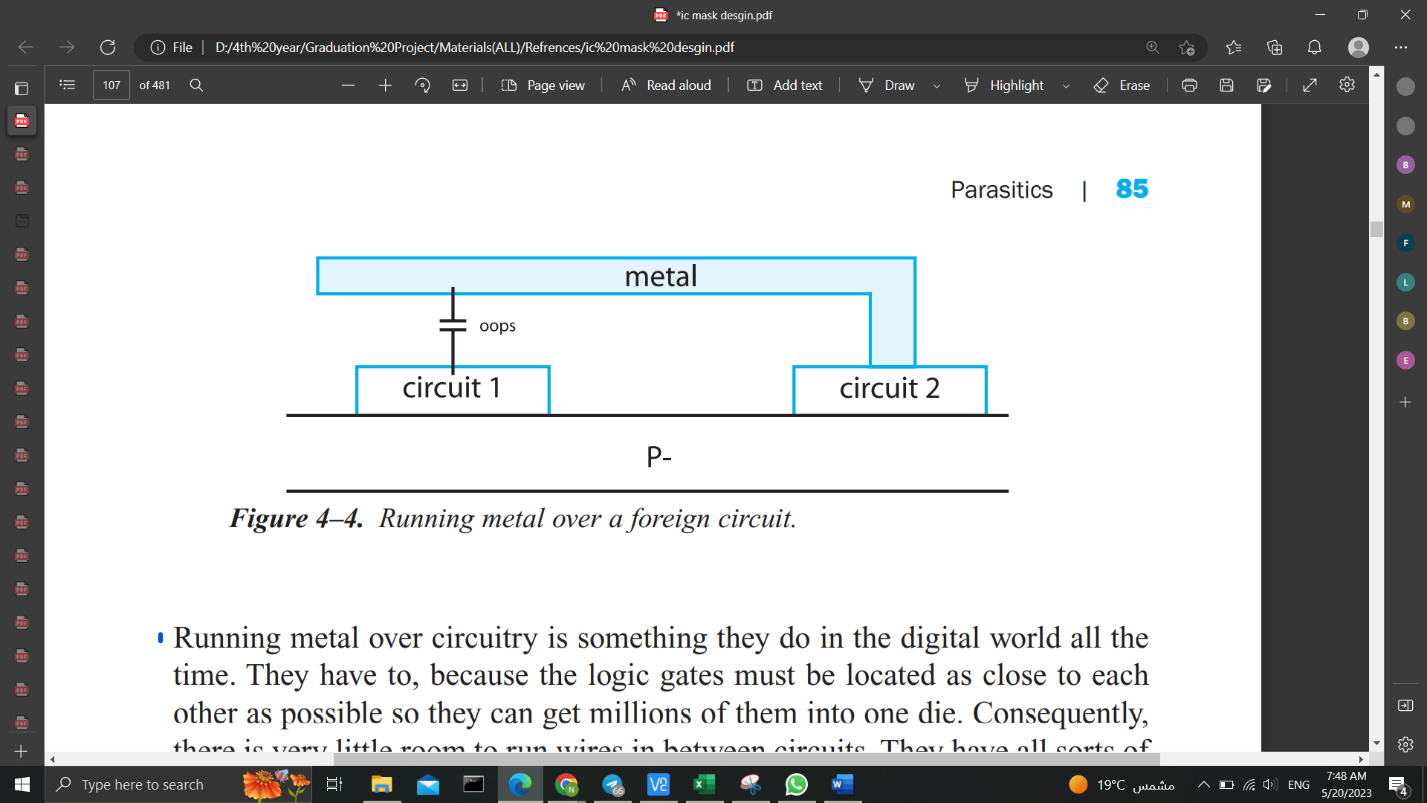


Figure. 3.4. Running metal over a foreign circuit

Running metal over circuitry is something they do in the digital world all the time. As they have to, because the logic gates must be located as close to each other as possible so they can get millions of them into one die. Consequently, there is very little room to run wires in between circuits. So, they have all sorts of metals running over the top of each other. Then there will be parasitic capacitance to their inverters, NAND gates, flip-flops, and so on.

Then assume there can be times when you will have critical wires in a digital circuit that are very sensitive to noise. However, the auto-router says, will put that wire anywhere it well feels like. After all, the auto-router is not paid to think, but just to route. And route it will, regardless of the consequences.

*While with analog circuits*, we typically want to keep sensitive signals away from each other. So, if we had a chip with wires all over the place, it may not work as well as if we had the individual circuits spaced away from each other. With no wiring going over the circuits, just wiring in between the circuits, the parasitics are much more controlled. ***You can kill your chip just by letting the auto-router place your wires without supervision.***

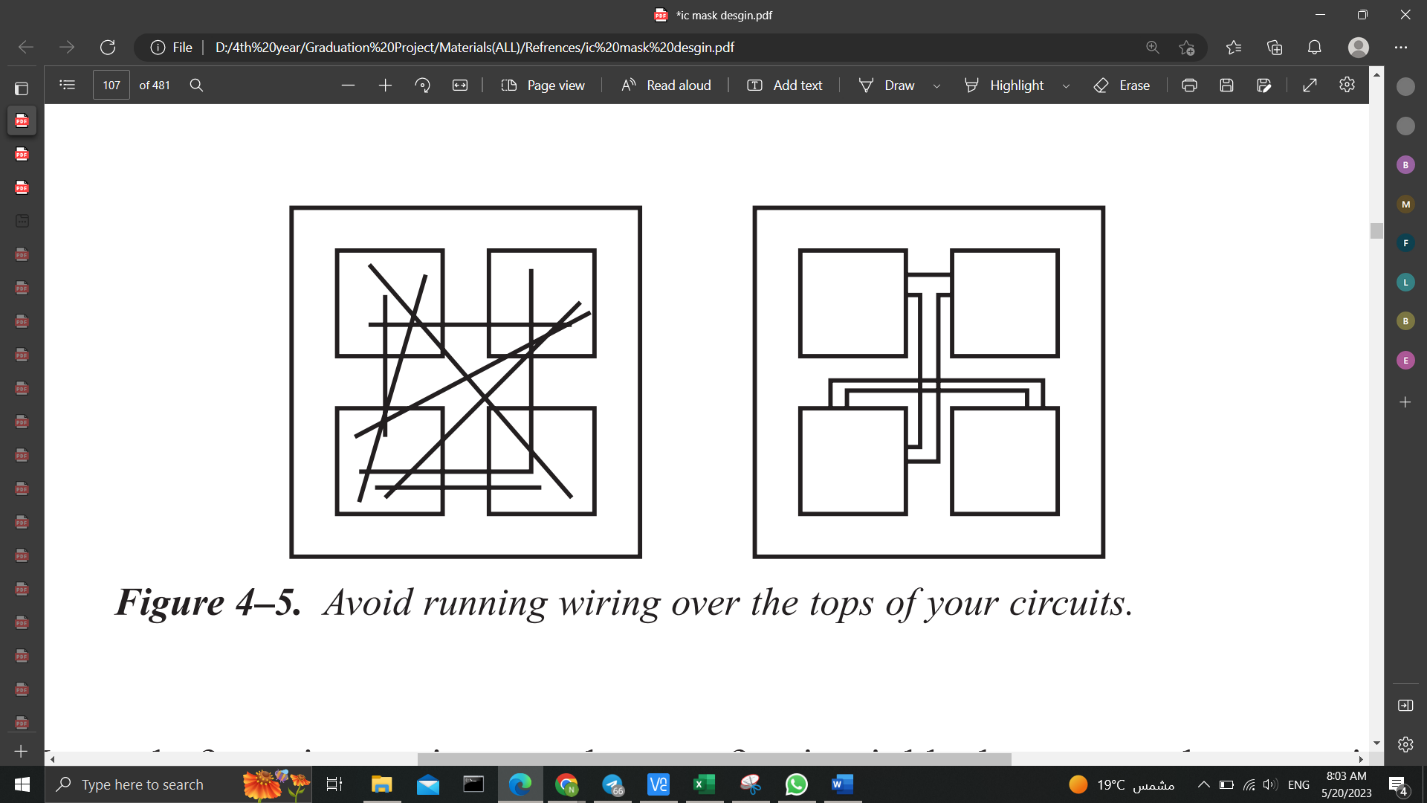


Figure. 3.5. Avoid running wiring over the tops of your circuits

Other way instead of running a wire over the top of a circuit block, is that we may have to wire entirely around a block as it’s a very sensitive node.

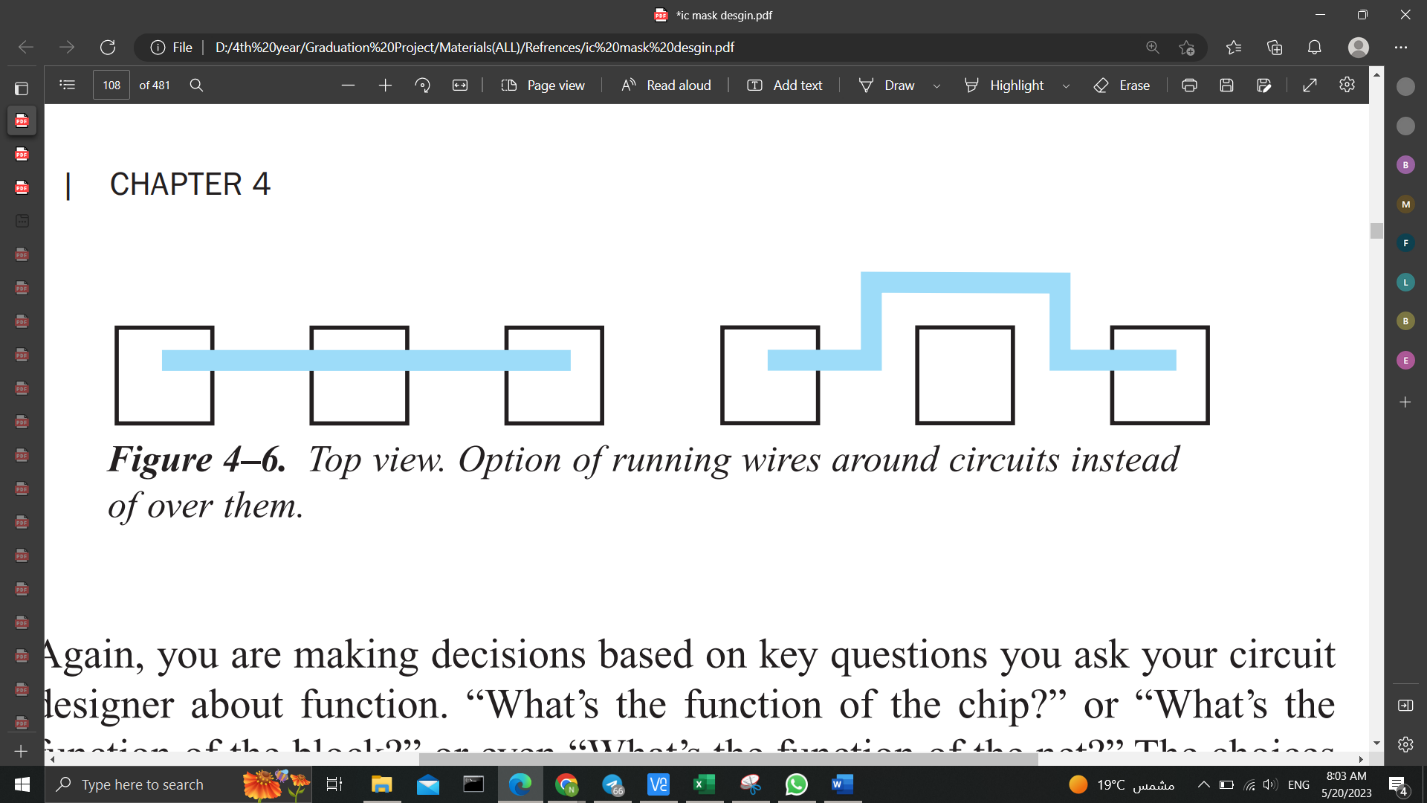


Figure. 3.6. Top view. Option of running wires around circuits instead of over them.

Once again, we are making decisions based on key questions you ask your circuit designer about function. such as “What’s the function of the chip?” or “What’s the function of the block?” or even “What’s the function of the net?” The choices you make depend on what the chip is doing. You may just not care about parasitic capacitances with some functions, with others you do.

When we are just designing low-level cell blocks, then the choices are more straightforward. But, when we begin to wire those cell blocks to each other, we have to ask a bunch of questions about an individual wire. which is very different from the digital world where 90% of the wiring is thrown together and who cares about the function.

But we mustn’t forget that, this is an oversimplification, of course, but the point is to let the circuit designer lead you. Ask about all levels of function. After all, you have to know.

1. **Parasitic Resistance**

Another parasitic mentioned at the beginning of this chapter is the *parasitic resistance*. Each wire has a parasitic resistance associated with it. And again, our handling of this parasitic depends on what the circuit does. This time we concentrate on our second question, “How much current does it handle?”. (Saint & Saint, 2002, p. 86).

If we recall, we looked at current densities to see how the amount of current affected our wiring width choice. In addition to wiring width choice, current affects cell-to-cell wiring choices as well.

* 1. **Calculating IR Drops**

The power supply in the chip is distributed uniformly through metal layers (Vdd and Vss) across the design. These metal layers have finite amount of resistance. Current begins to flow through the metal layers when voltage is applied to these metal wires, and some voltage is lost as a result of the resistance of the metal wires and current. It is known as an *IR drop*. (Shubham, 2023).

*How the timing is affected*: The Signal Integrity effect known as IR Drop is brought on by wire resistance and current drain from the Power (Vdd) and Ground (Vss) grid. Ohm's law states that V=IR. An unacceptable voltage drop may occur if the wire resistance is too high or the current flowing through the metal layer is greater than expected.

The power supply voltage drops as a result of this unacceptable voltage drop. This indicates that the cells are not receiving the necessary power across the entire design. Due to this, performance suffers and noise susceptibility increases. (Shubham, 2023).

Let us assume we have a wire that runs from one cell to another cell, which must handle 1 milliamp of current.

We look through our process manual to find the current density capability for this wire. We see that the metal we want to use can handle 0.5 milliamps per micron. That number tells us that we need to make that wire a minimum of 2 microns wide if we expect it to handle 1 milliamp.

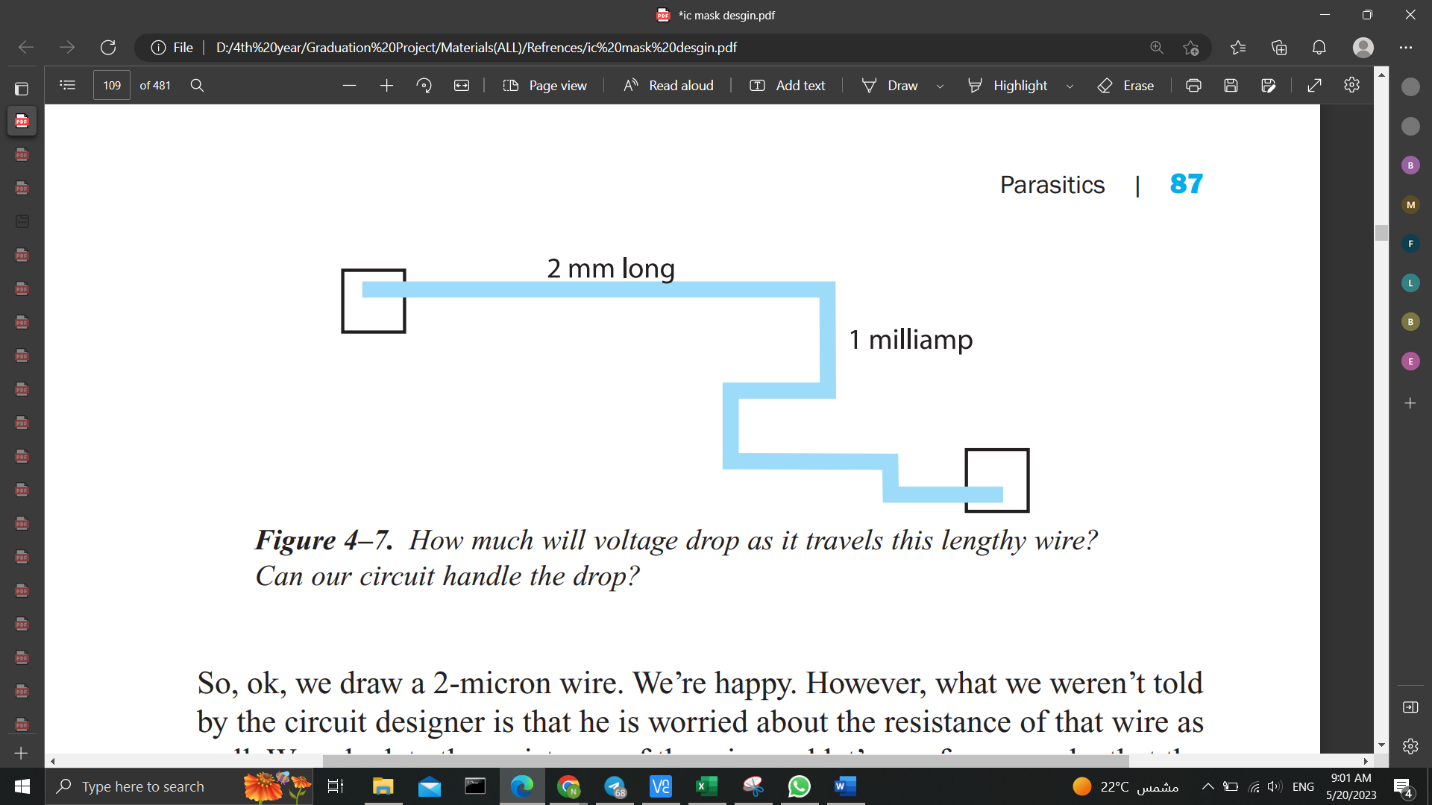


Figure. 3.7. How much will voltage drop as it travels this lengthy wire? Can our circuit handle the drop ?

So, yes, we draw a 2-micron wire. We’re good now! However, what we weren’t told by the circuit designer is that he is worried about the resistance of that wire as well. We calculate the resistance of the wire and let’s say, for example, that the length of our wire from one side to the other is 2 millimeters long. Being 2 microns wide, that equals 1000 squares. (Dividing length by width gives you the number of squares.)

Knowing the number of squares in our wire, we go to our process manual to find the resistance of that particular metal in ohms per square. We read that this metal is 50 milli-ohms per square. So, the resistance equals 1000 squares times 0.05 ohms per square.

The resistance through the wire is . Fifty ohms is a significant resistance. That wire is carrying . Using VIR, you calculate that the voltage drop across that wire is () times . That is a drop.

The difference in voltage level due to the current in this one piece of wire, is . If the circuit at the other end of the wire is sensitive to voltage offsets, then we have trouble. So again, it’s a case of going back to our circuit designer and saying, “we’re just finishing up this chip. I’ve got this really long wire from one side of the chip to the other. You told me it was taking 1 milliamp, so I’m getting a 50-millivolt drop, is that too much?”. But then the circuit designer will say, “that’s huge! That’s enormous! And he is sorry since he forgot to tell you that he needs a maximum of a 10-millivolt drop on that wire or the circuit won’t work properly.” That means we have to make our wire 5 times wider. So, instead of running our 2-micron wire, we apparently need a 10-micron wire. That will lower the drop to only 10 millivolts, which is within the requirements for this particular cell. these resistance parasitics typically manifest themselves in power wiring because power supply currents are usually pretty big. You can have 20 to 30 milliamps in one power supply. If you have a lot of circuits all connected to the same power supply, it needs to be sized to handle the right amount of current.

* 1. **Wiring Options**

We need to know the IR drop limitations and the amount of current flowing in your circuit. When we look at our top-level circuit, we may realize we have to split our power supply wiring into multiple pieces of wire just to handle these conditions. In Fig. 3.8, there is an array of circuits. Their power supply runs along from the bond pad into each circuit as shown. Our circuit designer tells us that the currents for the various blocks are , , , , , and , as noted.

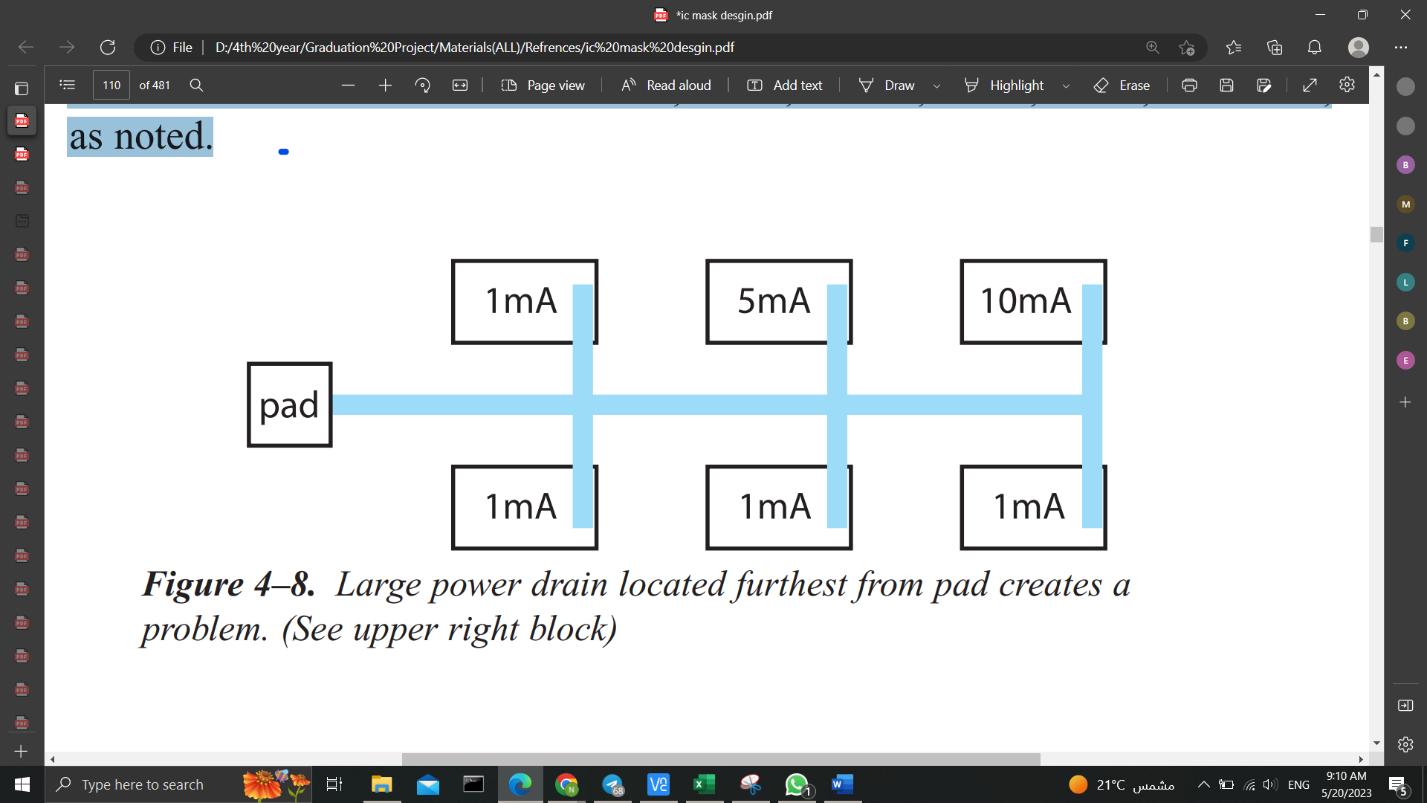


Figure. 3.8. Large power drain located furthest from pad creates a problem. (See upper right block)

It appears we have a total of 19 milliamps all coming in from the outside world through the pad on the left. Unfortunately, the block needing the most current is furthest from the pad. We could size our metal, all the way back to the last block, based on a total current of 19 milliamps. Let’s use our 0.5-milliamp-per-micron example for our wire. In that case, the wire width we need is 38 microns to be reliable. (Total amps divided by amps per micron.)

*Just give yourself a big fat chunk of metal. The whole thing is 38 microns wide.*

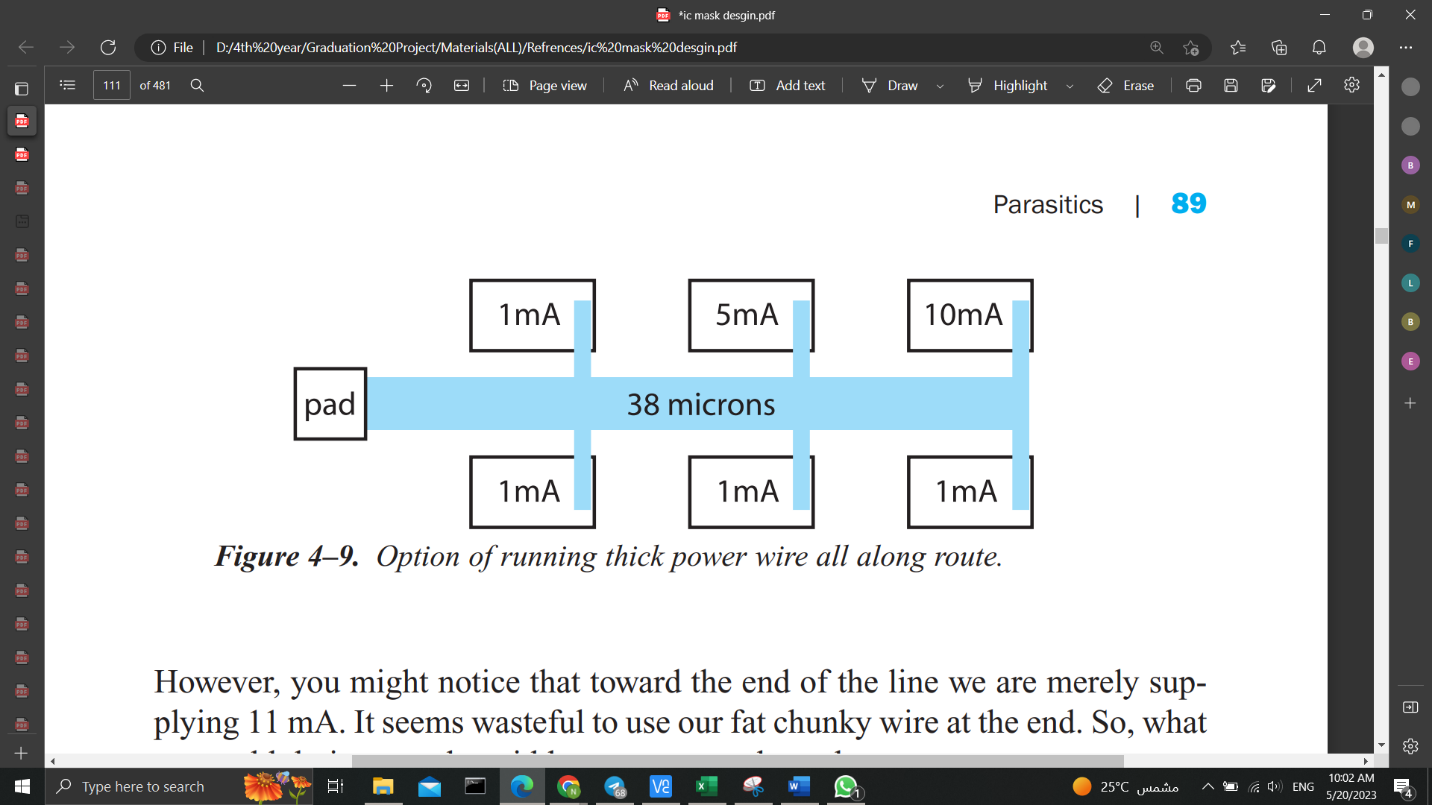


Figure. 3.9. Option of running thick power wire all along route

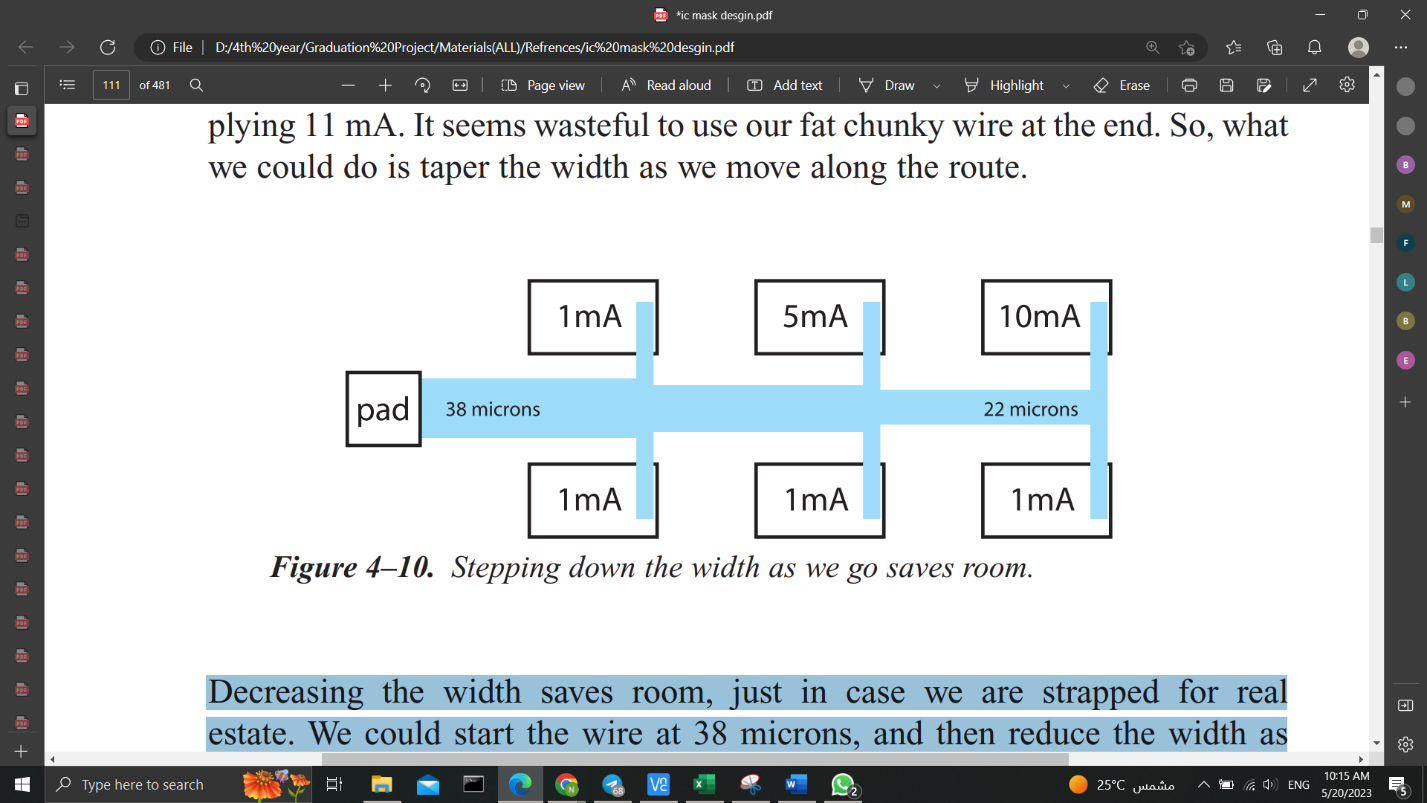
However, we might notice that toward the end of the line we are merely supplying 11 mA. It seems wasteful to use our fat chunky wire at the end. So, what we could do is taper the width as we move along the route.

Figure. 3.10. Stepping down the width as we go saves room

Decreasing the width saves room, just in case we are strapped for real estate. We could start the wire at 38 microns, and then reduce the width as needed.

There is another option. Why not bring the high current path back to the bond pad independently from the other wiring? You may need to use this option because you can get voltage drops caused by the 10-mA current that affect all the other blocks on the supply. This technique, of course, requires the chip real estate above the array of blocks.

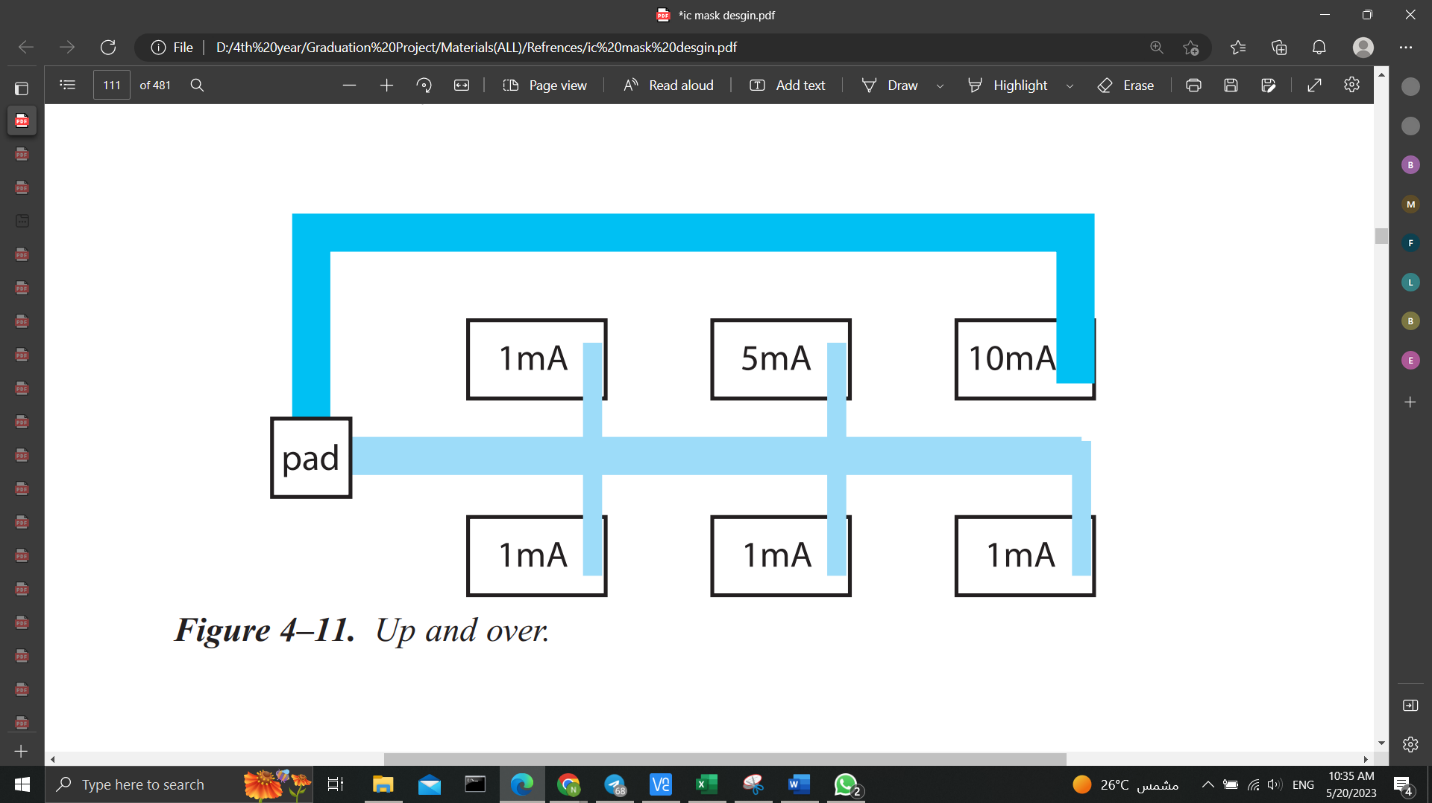
here are all sorts of options. Which method you use depends on the requirements of the circuit, which is based on the circuit function, and on what you’ve been asked to do.

Figure. 3.11. Up and over.

Hopefully you are seeing that knowing a bit about the way the circuit works affects your layout choices. Mask design is not just a case of hooking things up and hoping for the best.

**Rule of Thumb**: If your IR drop is bigger than 10 millivolts, check with your circuit designer.

In order to **reduce parasitic resistance**, make sure that you use the thickest metal. You can usually find the thickness of a metal in the process manual. If the metal thickness is not explicitly stated, then the metal resistance usually is. ***The thickest metal has the lowest ohms per square value.*** If your metals all have the same thickness, then you can sandwich chunks of metal on top of each other, as in Fig. 3.12.

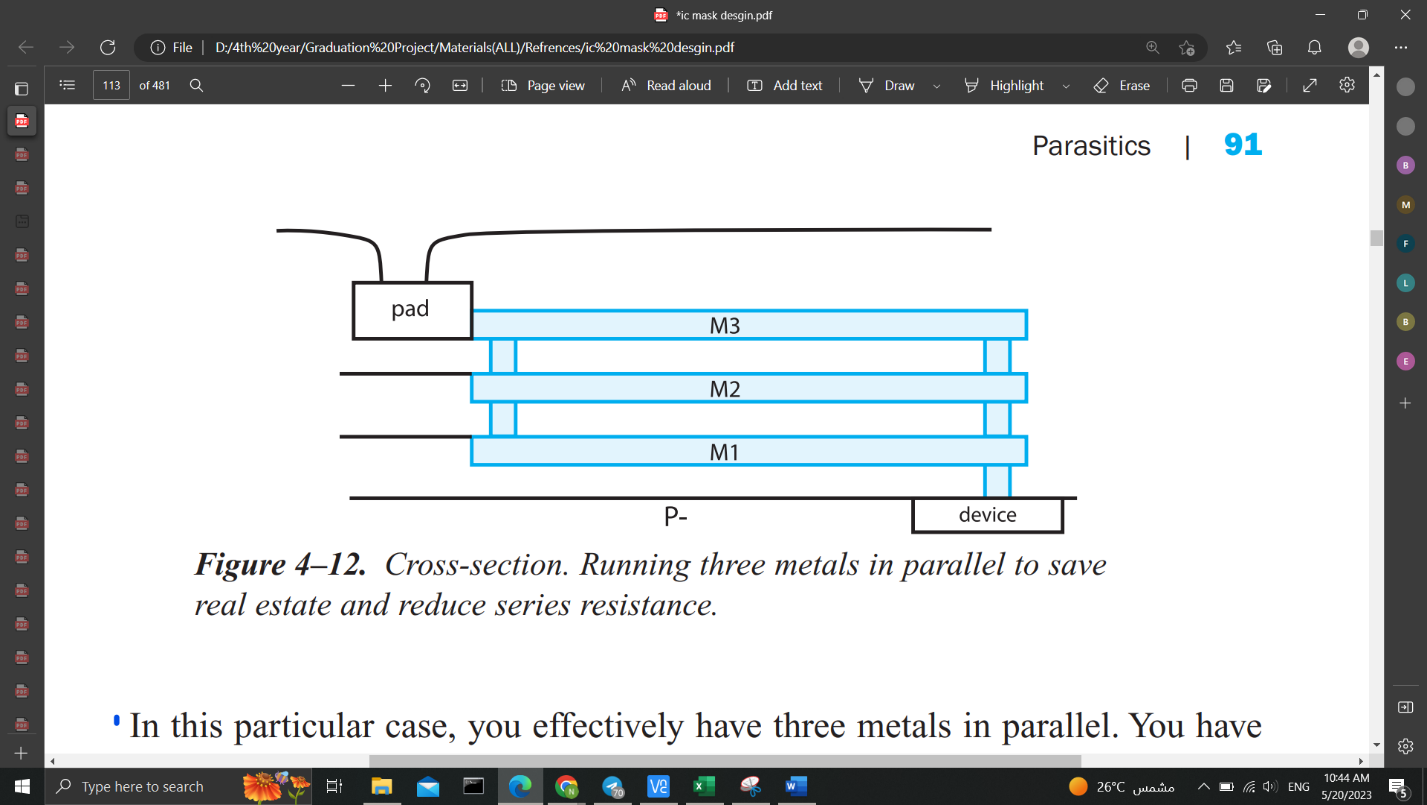


Figure. 3.12. Cross-section. Running three metals in parallel to save real estate and reduce series resistance.

In this particular case, you effectively have three metals in parallel. You have reduced the resistance by a factor of 3 for this wire because the current path is shared. In very high current situations, you may do your current density calculations and find, for example, that in order to be reliable, you need a wire 500 microns wide! Running strips in parallel is a good technique to reduce the resistance of high current paths and save yourself some space.

1. **Parasitic Inductance**

When you work with really high frequency circuits, the wires in your circuit start to have a parasitic inductance as well. The way to handle parasitic inductance is to try to model it, so that the inductance is calculated as part of the circuit.

Work with your circuit designer right away. Try to develop a floorplan of the chip very early so that the circuit designer can see how long the wires will be. He will incorporate some estimates of the inductances involved.

You may have to choose wires that are much wider than expected. You may have to leave room around certain wires because they are very inductive and very wide. You do not want them to inductively couple into other parts of the circuit. (Saint & Saint, 2002).

1. **Interconnect Parasitics**

Having presented parasitic effects *in the bulk*, e.g., Substrate Debiasing, Injection of Minority Carriers (won’t be discussed here), latchup (will be discussed latter) and *on the surface of silicon,* e.g., Parasitic channel effects, Hot carrier injection (won’t be discussed here), we now discuss parasitic effects *in the interconnect layers*. Again, our goal is to show how these effects can be suppressed through appropriate layout measures. (Lienig & Scheible, 2020).

*The real interconnects are not perfect short-circuits*, in general, there is a line resistance per unit length R`, a line inductance per unit length L`, an insulator capacitance per unit length C`, and an insulator conductance per unit length G` along a conductor. These primary line constants are illustrated as lumped parasitics R, L, C and G in the equivalent circuit diagram for a two-wire conductor in Fig. 3.13 (left). The circuit substrate can also assume the role of the second (bottom) conductor.

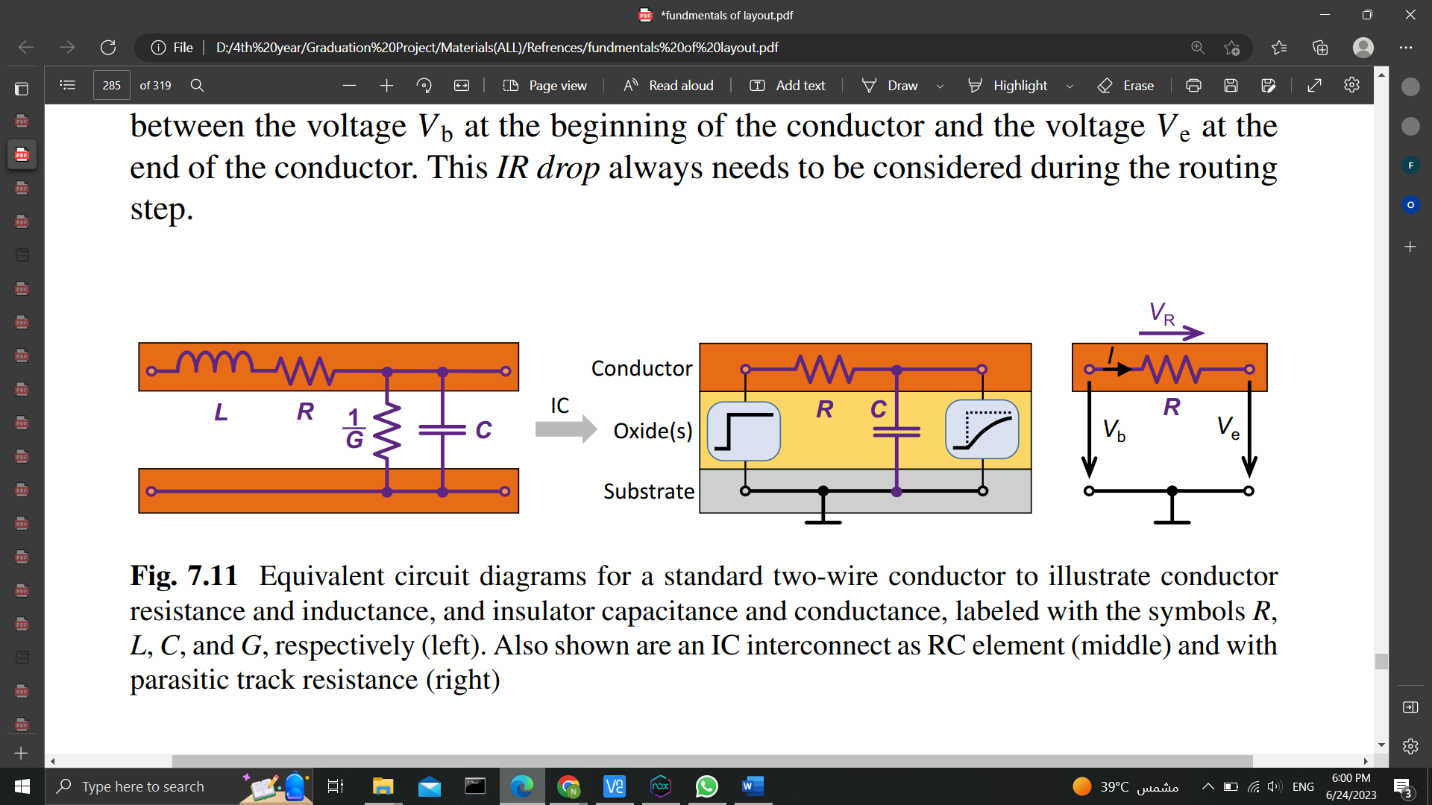


Figure. 3.13 Equivalent circuit diagrams for a standard two-wire conductor to illustrate conductor resistance and inductance, and insulator capacitance and conductance, labeled with the symbols R, L, C, and G, respectively (left). Also shown are an IC interconnect as RC element (middle) and with parasitic track resistance (right).

Due to the extremely small dimensions, we can disregard the self-inductance on a chip as long as the frequencies do not exceed the GHz range. Due to the excellent isolation properties of the oxides, the insulator conductance per unit length is typically negligible as well. On a chip, however, the parasites R and C play important roles (Fig. 3.13, middle). (Lienig & Scheible, 2020).

* 1. **Line Losses**

In the beginning, we will only take into account the parasitic track resistance R (Fig. 3.13, right), which is determined as follows:

(xx.1)

with line length l, interconnect width w, and sheet resistance . Thermal loss I2R is caused by this resistance R to the current I flowing in the conductor. Additionally, it results in a potential drop IR in the line, which is the difference between the voltages at the conductor's beginning and at its conclusion. This IR drop must always be taken into account during the routing step. If the current I is known during layout design, changing R can always change the IR drop. According to Eq. (3.1), the layout designer can modify the values of line length l, interconnect width w, and sheet resistivity R (depending on the layer selected). IR drops greater than should generally be checked at all times. Additionally, the placement of the devices should be optimised in this regard because the line length l greatly depends on the locations of the pins that need to be connected. Therefore, in order to avoid having to make the line width w too wide, devices that have high current flow between them should be placed as close to one another as possible. Generally speaking, the width w should be chosen so that the line's current-carrying capacity is sufficient.

* 1. **Signal Distortions**

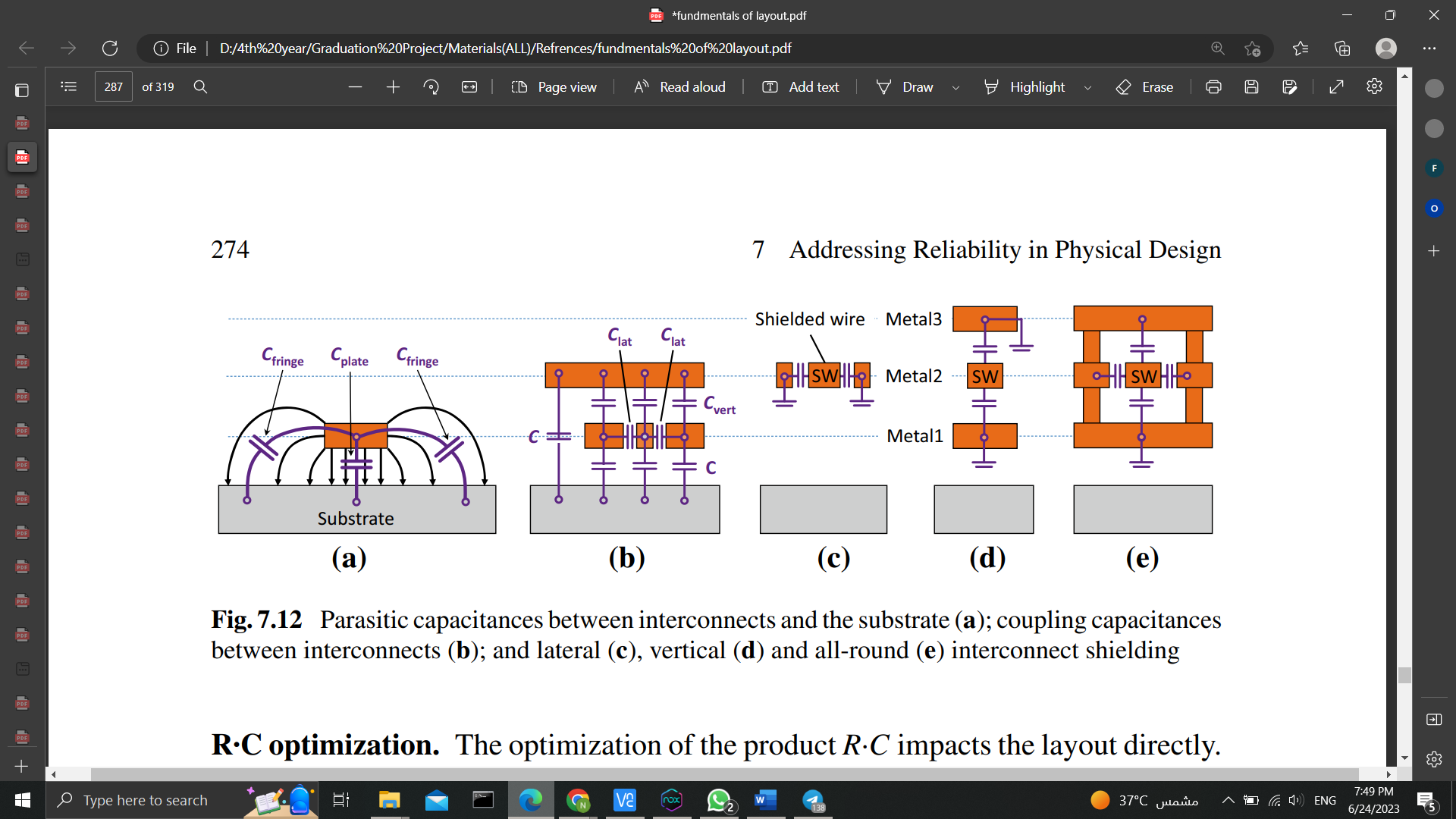
Every interconnect on a chip has a significant parasitic capacitance per unit length C to the chip substrate because of the thin deposited layers on the chip. The equivalent circuit diagram in Fig. 3.13 (middle) shows a condensed version of this scenario with a lumped capacitance C. For each signal sent through the interconnect, the resistor R (also known as the RC element) must charge the capacitor C. For an ideal step function as the input signal at the line's beginning, see Fig. 3.13 (middle). By the time the signal reaches the end of the queue, it has been delayed and distorted. RC, also referred to as the time constant of the RC element, serves as a measure of the time delay (67% of the final value is reached after this time). How can we alter the product R·C in the layout?

The substrate can be thought of as the counter-electrode to each interconnect's capacitor electrode. The well-known parallel plate capacitor equation (3.2) is as follows:

(3.2)

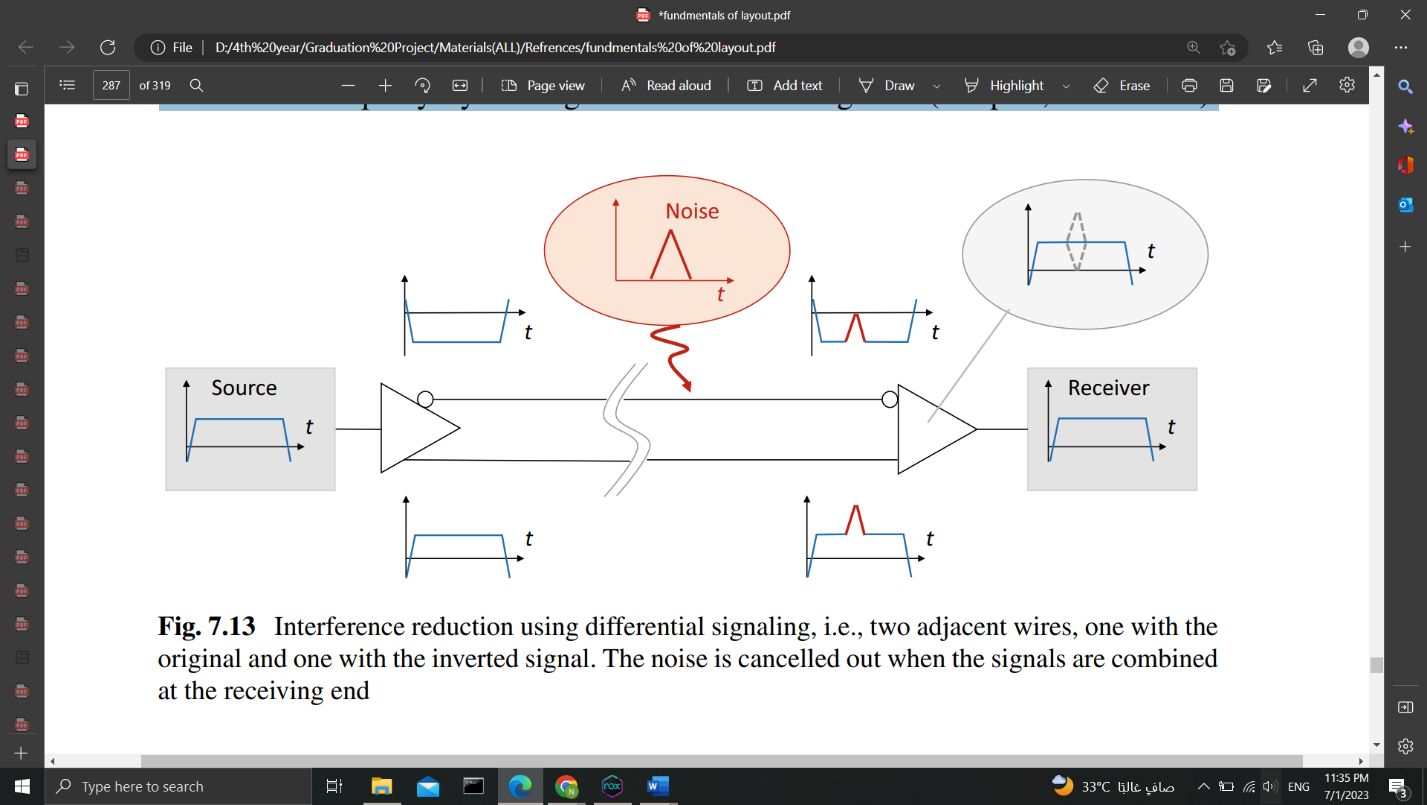
The equation demonstrates that C is inversely proportional to the oxide layer thickness d and scales with the wire surface area A (i.e., with the width w and length l). Because of the lower metal layers' reduced value of d due to their proximity to the substrate, they have higher parasitic capacitances than the upper layers.

But eq. (3.2) does not take into account the fringe fields, so it cannot accurately calculate the capacitance of a chip interconnect. (Due to w d and l d, the fringe fields on a typical parallel-plate capacitor are insignificant.) using a chip the lateral fringe fields significantly contribute to C and interconnect. For typical narrow (i.e., small-width) interconnects (e.g., w 2 m for Metal1, w 4 m for Metal2), the capacitance per unit length C fringe resulting from the fringe fields is greater than the plate capacitance per unit length C plate (Fig. 3.14a).



*Figure. 3.14 Parasitic capacitances between interconnects and the substrate (a); coupling capacitances between interconnects (b); and lateral (c), vertical (d) and all-round (e) interconnect shielding*

**The following is a way of the key principles for physical design distortion reduction:**

**Differential-pair routing: Another cause of signal distortions on wires is external disturbances. By inverting the signal and sending it in a second wire parallel to the original signal to the receiver, sensitive analogue signals can be sent over long distances reasonably securely (Fig. 3.15). By placing both interconnects close together, it is intended to ensure that disturbances affect them equally.

*Figure. 3.15 Interference reduction using differential signaling, i.e., two adjacent wires, one with the original and one with the inverted signal. The noise is cancelled out when the signals are combined at the receiving end.*

* 1. **Crosstalk**

A lot of coupling capacitances are produced between laterally adjacent interconnects (Clat) and vertically adjacent interconnects (Cvert) in addition to the capacitances to the substrate (see Fig.3.14b). These capacitances disrupt the electronic circuit by causing signal crosstalk. The distances between interconnects are getting closer as IC downscaling of feature sizes advances, and these parasitics are getting bigger. Modern Damascene processes can create cross-sections with extremely high and narrow interconnects (Fig.3.14c). As a result, *the quantity Clat is more important than Cvert in cutting-edge processes than in traditional processes*. (Lienig & Scheible, 2020).

**The following is a summary of the key principles for physical design crosstalk reduction:**

1. Digital and analogue signal isolation: Digital signals typically have sharp edges that contain high frequencies. Due to the AC reactance RC = |1/ωC|, these edges severely perturb capacitively coupled interconnects. Therefore, sensitive analogue signals should be routed apart from digital signals, such as sensor signals. The biggest offenders in this regard are clock nets.
2. Shielding: Crosstalk can be reduced by surrounding interconnects with grounded interconnects if lines cannot be physically isolated or if this isolation is insufficient. As a result, the lines are protected from disruptions. The three shielding configurations are: all-around, all-lateral, and vertical only (see Fig. 3.14c-e).
3. Avoiding minimum spacings: The lateral interconnect spacing within a layer can be changed, whereas the ILO (interlevel oxide) thickness cannot be. If the footprint permits, it is a good idea to forgo using minimum spacings for crucial interconnects (both for perpetrators and victims). It is best practice to use any remaining whitespace after routing all nets to increase or decrease wire spacing.

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3. Saint, J., & Saint, C. (2002). IC Mask Design. McGraw-Hill.
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